REMARKS

In response to the **NOTICE OF OMITTED ITEM(S) IN A NONPROVISIONAL APPLICATION** dated July 31, 2001, the specification has been amended to cancel all references to omitted Fig. 5 and the page in the drawings labeled Fig. 5 has been canceled. The Applicants accept the application as deposited in the United States Patent & Trademark Office, and thus the filing date as the date of deposit of the application. The response is provided prior to the mailing of the first Office Action in an effort to avoid delays in the prosecution of the application.

VERSION OF AMENDMENTS MADE TO SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Fig. 3 depicts a functional block diagram of a processor configuration for processing bit transfer operation instructions according to embodiments of the present invention; and

Fig. 4 depicts a method of processing bit value transfer operation instructions according to embodiments of the present invention.[; and

Fig. 5 depicts a table of bit value transfer operation instructions according to embodiments of the present invention.]

According to embodiments of the present invention, a method and a processor for processing bit value transfer operation instructions are provided. The bit transfer operation instructions themselves include four instructions, each for selecting a bit value contained in a source bit position of a data memory location and writing the bit value to a destination bit position of another data memory location. Moreover, the instructions specify a source bit position of a data memory location containing a bit value to select, a destination bit position of another data memory location to write the bit value, and the data memory location of an operand from which to read or write the bit value. [The instructions are shown in Fig. 5].

In order to describe embodiments of bit value transfer operation instruction processing, an overview of pertinent processor elements is first presented with reference to Figs. 1 and 2. The bit transfer operation instructions and instruction processing is then described more particularly with reference to Figs. 3-4[5].

Fig. 3 depicts a functional block diagram of a processor for processing bit value transfer operation instructions according to the present invention. Referring to Fig. 3, the processor includes a program memory 300 for storing instructions, such as the bit value transfer operation instructions [depicted in Fig. 5]. The processor also includes a program counter 305 which stores a pointer to the next program instruction that is to be fetched. The processor further includes an instruction register 315 for storing an instruction for execution that has been fetched from the program memory 300. The processor may further include pre-fetch registers (not shown) that may be used for fetching and storing a series of upcoming instructions for decoding and execution. The processor also includes an instruction decoder 320, an arithmetic logic unit (ALU) 325, registers 345 and a status register 350.

The bit value transfer operation logic 340 may be part of or separate from the ALU logic 335. The bit transfer operation logic, however, is logically separate from the ALU logic 335 and is activated upon the execution of [one of] a bit value transfer operation instruction [shown in Fig. 5]. The bit value transfer operation logic 340 may receive one or more operands from the registers 330. The operands may include a data word, a data byte and a data bit. The bit transfer operation logic may execute bit value transfer operation according to the instructions decoded by the instruction decoder on an operand contained in registers 345, status register 350 and/or an address location in data memory 355.

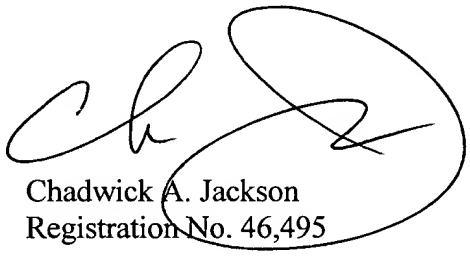
In this regard, when a bit value transfer operation instruction[, such as one of those depicted in Fig. 5,] is presented to the instruction decoder 320, the instruction decoder generates control signals which cause the ALU to fetch a source operand from the registers 345 or from the

data memory 355 and which cause the bit operation logic 340 to operate on the fetched source operand to produce a result in accordance with the instruction. For example, the control signals can cause the ALU to fetch a source operand from a data memory location, select a bit value in a bit position of the source operand at the data memory location, copy the bit value at the bit position and write the bit value to a destination bit position at another data memory location. Alternatively, the control signals can cause the ALU to fetch a source operand from a data memory location, select a bit value in a bit position of the source operand at another data memory location, copy the bit value at the bit position and write the bit value to a destination bit position at the initial data memory location. The result depends upon the instruction executed and the source operand as is explained below in more detail. After generating the result, the instruction decoder causes the result to be written back into the correct register 345 or memory location within the data memory 355.

CONCLUSION

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with this application to Deposit Account No. 19-5127 (18153.0033). A duplicate of this authorization is attached for the Finance Branch.

Respectfully submitted,
Swidler Berlin Shereff Friedman, LLP



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